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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,623	07/26/2004	Kuo-Chao Lin	12574-US-PA	4622

31561 7590 11/29/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PHAN, DEAN	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
11/29/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/710,623	LIN, KUO-CHAO	
	Examiner	Art Unit	
	Dean Phan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/06/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 09/06/2007 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

> Prior art of record does not disclose, "setting a parameter set group based on said reading table".

In response to argument, examiner respectfully traverses. It appears that the applicant is not interpreting the previous office action as intended by the examiner. According to examiner, a table is an arrangement of data. In column 3 lines 56-62 and further in column 5 lines 26-34, Futral discloses the step of establishing a table by **arranged two separate locations** for status storage location 244, and parameter storage location 243 within the memory 240. Further in Figure 3-6, Futral discloses the arrangement within one parameter storage (e.g. *parameter storage location 343*) where "src data stor loc base addr", "dest data stor loc base addr", "quantity of data", and "status stor loc base addr" are stored. In column 5 lines 40-44, Futral also discloses, "CPU 210 is able to **read** status storage location 244..." Therefore, the reading table is **the arrangement of the location** of each status storages and parameter storages to be stored within the memory 240 and **read** by the CPU 210.

Futral does disclose the step of "setting a parameter set group based on said reading table and moving said parameter set group to said area of said main memory". First, Futral discloses at least two parameter set groups in figure 3-6, (e.g. status

storage 344, parameter storage 343). Moreover, in column 3 lines 54-66 and further in column 5 lines 20-35, Futral discloses,

"CPU 210 **writes various parameters** of the transfer to take place into memory locations within parameter storage location 243 allocated within system memory 240. Such parameters could include, but are not limited to, the *starting addresses* of data storage locations 246 and 266, *a value* indicating the quantity of data to be transferred, and *a value* indicating that the status of the transfer is to be provided at status storage location 244 allocated within system memory 240".

Apparently, to "write these various parameters" into memory location, the CPU has to **set** a parameter set group by at least **having** values for these parameters and **locating** the locations where these parameters are going to be stored in the memory based on said arrangement. The CPU then "moves said parameter set group to said area of said main memory" by **writing** the parameters **into memory location**. Therefore, Futral discloses the above limitations.

The rejection is maintained.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (U.S Pub# 2005/0160223), in the view of Futral et al (U.S Pat# 7,120,708).

As to claim 1, Chen et al teach a direct memory access method for a card reader

(abstract; *card reader/flash card exchanger),* said card reader (Fig 2 card exchanger 38) including a direct memory access controller (Fig 2 microcontroller 30, par. 57) and being coupled to a system (host PC 10), said system including a main memory and a control software (PC *has a memory and OS software in order to operate),* said system executing a driver program (Fig 6, abstract, par. 11) to control said card reader. Chen et al also teach sending out an interrupting signal to said system (par. 36). Chen et al do not teach the method comprising from step a to step g. However, in the same field of art, Futral et al teach a direct memory access system (abstract) comprising:

a. allocating an area of said main memory (Fig. 1, col 3 lns 56-62);

b. establishing a reading table (Fig. 3, col 4 lns 11-19, col 5 lns 26-34; *Status storage location in memory functions as a reading table. The arrangement of these locations in combination with others such as parameter storages is a table that is read by CPU)* via said control software (col 5 lns 50-52);

c. setting a parameter set group based on said reading table (col 3 lns 54-66, col 5 lns 20-35; *The CPU has to* ***set*** *a parameter set group by* ***having*** *values for these parameters and* ***locating*** *the locations where these parameters are going to be stored based on said arrangement*) and moving said parameter set group to said area of said main memory (Fig. 10 step 1010, col 12 lns 5-10);

d. acquiring an initial address of said parameter set group (step 1020);

e. reading a parameter value from said initial address (col 12 lns 10-13);

f. using a direct memory access method to move data based on said parameter value (step 1030);

g. repeating said steps e and f before reading all said parameter values (step 1050);

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Chen and Futral et al. in order to reduce the time of data transfer. (see col 1 lns 53-61).

As to claim 2, Chen and Futral et al teach the method of claim 1 with further: said reading table is established based on a block status recording area (Futral, col 3 lns 34-48) of a memory card (Chen, Fig. 2 memory card 22, 26, 32, 36).

As to claim 3, all same limitations are listed in claim 1 with further: said parameter set group is moved by said driver program (Futral, col 3 lns 56-61).

As to claim 4, all limitations are listed in claim 1 with further: said parameter set group at least includes a parameter set (Futral, col 3 lns 66-col 4 lns 5).

As to claim 5, all same limitations are listed in claim 1 with further: said initial address of said parameter set group is provided by said driver program to said direct memory access controller (Futral, col 1 lns 25-30).

As to claim 6, all same limitations are listed in claim 1 with further: each parameter set of said parameter set group includes an origin address of said data (Futral, Fig 3 *src data storloc base addr)* and a target address of said data (Futral, *dest data stor loc base addr).*

As to claim 7, all limitations are listed in claim 1 with further: said parameter set group at least includes a plurality of parameter sets (Futral, Fig *6 parameter storage*

location 643a-c) and each of said plurality of parameter sets assigns a direct memory access range (Futral, Fig *6 quantity of data).*

As to claim 8, all limitations are listed in claim 7 with further: at least one of said plurality of parameter sets includes a parameter indicating an initial address of a following parameter set (Futral, Fig. *6 next param stor loc base addr).*

As to claim 9, Chen et al teach a method for programming a direct memory access controller (Fig 6) for a card reader (Fig 2 card exchanger 38), said card reader including the direct memory access controller (Fig 2 microcontroller 30, par. 57) and being coupled to a system (host PC 10), said system including a main memory and a control software *(PC has a memory and OS software in order to operate),* said system executing said driver program to control said card reader (Fig 6, abstract, par 11). Chen et al do not teach said control software establishing a reading table, said driver program setting a parameter set group based on said reading table and moving said parameter set group to an area of said main memory, and from step a to step d. However, in the same field of art, Futral et al teach a method for programming a direct memory controller wherein the program establishing a reading table (col 4 lns 11-19, col 5 lns 26-52; *Status storage location in memory functions as a reading table. The arrangement of these locations in combination with others such as parameter storages is a table that is read by CPU),* said driver program setting a parameter set group based on said reading table (col 3 lns 54-66, col 5 lns 20-35; *The CPU has to* ***set*** *a parameter set group by* ***having*** *values for these parameters and* ***locating*** *the locations where these parameters are going to be*

stored based on said arrangement) and moving said parameter set group to said area of said main memory (Fig. 10 step 1010, col 12 lns 5-10). The said method comprising:

a. said driver program (col 3 lns 56-65, col 12 lns 10-13; *The instructions is executed by CPU)* providing an initial address of said parameter set group to said direct memory access controller (Fig. 10 step 1020);

b. according to said initial address *(base address),* said direct memory access controller reading a parameter value (Fig. 6, col 9 lns 37-51), which has not been read *(The DMA controller obtains the base address of next parameter from the previous one),* from said parameter set group (Fig 6 parameter storage location 643a-c) in a predetermined sequence *(parameters link to each other);*

c. said direct memory access controller using a direct memory access method to move data based on said parameter value (Fig 6, Fig 10 step 1030; *Using the value in the parameters to move data);* and

d. repeating said steps b and c before reading all said parameter values (step 1050).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Chen and Futral et al. in order to reduce the time of data transfer. *(see* col 1 lns 53-61).

As to claims 10-14, all same limitations are listed in claim 9 with further limitations in claims 2, 4, 6-8.

Examiner's note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified

citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean Phan whose telephone number is (571) 270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571) 272 4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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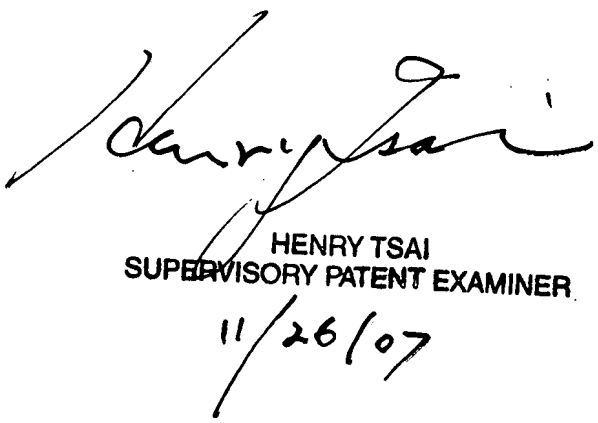

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SUPERVISORY PATENT EXAMINER
11/26/07